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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,059	11/07/2001	Nobuaki Tokushige	900-406	4809

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/986,059	TOKUSHIGE ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 16-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuller [U.S. Pat. 5,804,846] previously applied, in view of Buynoski et al. [U.S. Pat. 6,465,334] previously applied.

With respect to claim 16, Fuller (fig. 2E and cols. 3-4) discloses a semiconductor device comprising:

a metal gate electrode (231) provided on a semiconductor substrate (201) with the intervention of a gate insulating film (222), wherein gate insulating film (222) is located between the metal electrode (231) and a channel (307) of the transistor for which the gate electrode is provided;

a sidewall insulating film (221) provided on a side wall of the metal gate electrode;

source/drain regions (213, 214) provided in the semiconductor substrate for the transistor, the channel (307) being provided between the source/drain regions (213, 214); and

metal contact plugs (232, 233) provided on the source/drain regions;

wherein the metal gate electrode (231) is electrically isolated from the metal contact plugs (232, 233) by the sidewall insulating film (221) alone;

wherein the metal gate electrode (231) is partly or entirely composed of the same material as the metal contact plugs (232, 233);

wherein the metal gate electrode (231) and the metal contact plugs (232, 233) have the same height.

Fuller does not disclose that the metal gate electrode directly contacts an upper surface of the gate insulating film. However, Buynoski et al. discloses the metal gate electrode (128b) directly contacts an upper surface of the gate insulating film (125) (see fig. 16 and col. 5, lines 62-67; col. 6, lines 1-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the metal gate electrode directly contacts an upper surface of the gate insulating film as

taught by Buynoski et al. into the device of Fuller because metal gate electrodes have a greater conductivity than polysilicon electrodes and do not require complicated silicide processing in order to perform at high operational speeds (see col. 2, lines 39-42).

With respect to claim 17, Fuller disclose that an insulating film (241) is provided over both the metal gate electrode (231) and isolation regions (206) on opposite sides of the metal gate electrode, but is not provided over at least part of the source/drain regions (see fig. 2F and col. 4, lines 65-67; col. 5, lines 1-6).

With respect to claim 18, Fuller discloses that the metal gate electrode (231) comprises aluminum (see col. 20-24).

With respect to claim 19, Fuller discloses that no silicide layer is provided over the metal gate electrode.

With respect to claim 21, Fuller disclose that the metal gate electrode (231) and metal contact plugs (232, 233) are formed of the same material (see figs. 2D-2E and col. 4, lines 20-45).

4. Claims 20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuller [U.S. Pat. 5,804,846] previously applied, in view of Buynoski et al. [U.S. Pat. 6,465,334] previously applied as applied to claim 16 above, and further in view of Hieda [U.S. Pat. 6,072,221] previously applied.

Fuller substantially disclose all the limitations as claimed above except that conductive interconnects are provided over the respective metal contact plugs, and wherein at least portions of the conductive interconnects are in contact with respective vertically aligned sidewalls of the metal contact plugs. A conductive interconnection formed by a dual damascene process located over and contacting at least one of the metal contact plugs, wherein an upper conductive surface of the conductive interconnection is flat. However, Hieda discloses conductive interconnects (14) are provided over the respective metal contact plugs (11), and wherein at least portions of the conductive interconnects (14) are in contact with respective vertically aligned sidewalls of the metal contact plugs (11). A conductive interconnection (14) formed by a dual damascene process located over and contacting at least one of the metal contact plugs (11), wherein an upper conductive surface of the conductive interconnection (14) is flat (see fig. 7C and col. 7, lines 23-67; col. 8, lines 1-6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the conductive interconnection of Fuller by forming the conductive interconnection with the structure as set forth above because according to Hieda, such conductive interconnection would prevent an electrical short-circuit (see col. 7, lines 34-37).

Response to Arguments

5. Applicant's arguments filed 07/13/2005 have been fully considered but they are not persuasive.

Applicant argues that Fuller fails to disclose or suggest the metal gate electrode directly contacts an upper surface of the gate insulating film so that only the gate insulating film is located between the metal gate electrode and a channel of a transistor for which the gate electrode is provided.

This argument is not persuasive because the rejection of the invention as claimed is not based on anticipated, but rather, is based on obviousness. Thus Applicant 's arguments are arguments against the references individually but not proper arguments where references are applied in combination. It is noted that, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller,* 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, the teaching of Buynoski et al. discloses the metal gate electrode (128b) directly contacts an upper surface of the gate insulating film (125) (see fig. 16 and col. 5, lines 62-67; col. 6, lines 1-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the metal gate electrode directly contacts an upper surface of the gate insulating film as taught by Buynoski et al. into the device of Fuller because metal gate electrodes have a greater

conductivity than polysilicon electrodes and do not require complicated silicide processing in order to perform at high operational speeds (see col. 2, lines 39-42).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

7. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER